Design Tips: Standard Sync SRAM Standards - AN4019

Introduction

Some users have the impression that there is no standard among Standard Sync SRAMs. This technical note deals with standardization issues as they pertain to PC designs: designing with today’s parts, taking advantage of their features and avoiding redesign by taking into account all the JEDEC-defined features and options.

Changes Since Original Part Introduction

Since the Standard Sync architecture was introduced and standardized through the JEDEC committee, many other vendors have decided to design and manufacture 1-Mb, 2-Mb, 4-Mb, 9-Mb, 18-Mb, 36-Mb, and 72-Mb devices in x18, x32, x36, and x72 configurations. Most vendors have versions that vary from the original JEDEC pin assignment. The original JEDEC standard has undergone changes since its introduction, and Figure 1 illustrates the final standard.

The changes from the original standard are: remove PDIS from pin 87; add GW on pin 88, BWE on pin 87, FT on pin 14, MODE on pin 31 and ZZ (optional) on pin 64. Not all vendors support every function on these devices. But reserving a position for all anticipated functions allows designers to lay out their PCBs so that any vendor’s part will work in their application. If a vendor chooses not to implement a function, the corresponding pin is a no connect and will not conflict with whatever logic level the pin has been tied to.

Benefits of New Signals

MODE signal in Cypress devices permits the user to select the burst sequence (pin 31). This is a static input; therefore, its state may not be changed during device operation. A LOW on this input selects linear burst sequence. A HIGH selects interleaved burst sequence. Linear and interleaved burst operate differently when the starting address is odd. Linear burst sequence is a simple modula-4 up-counter with wraparound, whereas in interleaved burst, the least significant address bit toggles every cycle and the next significant bit toggles every other cycle. This is detailed in the device data sheets. The benefit to the manufacturer for supporting this input is that fewer part types have to be supported. The benefit to the user is that more design flexibility is permitted, allowing a variety of microprocessors or ASIC designs to be considered with no cost penalties.

Global Write (GW) synchronous input provides a means to perform a full bus-width Write to the SRAM using a single pin. It is valuable to cache controllers when performing a line fill, since line fills are always in integer numbers of the full bus.
width. ASIC designs benefit from the reduction of load. Prior to this input, the Byte Write signals must all be brought LOW to perform a full-width Write resulting in a load of four signals per 32-bit bus width. If GW input is not needed, it may be tied HIGH.

Byte Write Enable (BWE) synchronous input works as a logical OR with the BWx signals. The latter signals are ignored unless BWE is LOW. This signal permits direct connection of microprocessor byte enables to the Byte Write lines of the SRAM (Figure 2). This results in two major benefits: zero-wait-state Writes and ASIC pin-count reduction. Write cycles are faster because ASIC logic delays, I/O buffers, and extra PCB propagation delays are eliminated by directly connecting the microprocessor signals to the SRAM. Only a single critical path persists instead of eight input and eight output critical signal paths as is the case when the ASIC must translate the byte enables into byte writes for the SRAM (Figure 3). The single critical path is now converting the microprocessor Read/Write signal into a BWE input to the SRAM. This results in two major benefits: zero-wait-state Writes and ASIC pin-count reduction. Write cycles are faster because ASIC logic delays, I/O buffers, and extra PCB propagation delays are eliminated by directly connecting the microprocessor signals to the SRAM. Only a single critical path persists instead of eight input and eight output critical signal paths as is the case when the ASIC must translate the byte enables into byte writes for the SRAM (Figure 3). The single critical path is now converting the microprocessor Read/Write signal into a BWE input to the SRAM. The single path is easier to manage and can be done without inducing wait-states. The second benefit is pin-count reduction in the ASIC (i.e., cache controller). Previously, eight input and eight output signals were needed for Writes. Now, only eight bidirectional signals and two outputs are needed to replace the function of 16 lines: a net savings of six pins in 64-bit applications. Figure 2 and Figure 3 show the difference between systems that take advantage of GW and BWE and those that do not.

Flow-through (FT) input is another static input. Some vendors will implement this input to allow user selection of pipelined (FT = HIGH) or nonpipelined designs also called flow-through (i.e., no registers in series with device outputs). While vendor support of this additional mode-select input allows the same device to work in either regular or pipelined designs, many vendors do not plan to support it. Designers must strap the FT pin to the logic level appropriate for the design to ensure that a wide selection of sources will operate in the design.

Sleep (ZZ) input is available from Cypress. It will be included by some vendors to provide a way to put the SRAM into the lowest power standby mode (see I$BB2 specification in the data sheets). Currently, the clock must be stopped and all inputs held within 0.2V of VDD or VSS to lower the standby power to the lowest level possible. ZZ held HIGH in the Cypress device will cause the SRAM to enter into “sleep” mode in approximately two clock cycles in nonpipelined devices. Pipelined devices will take one extra clock cycle. After the device is “sleeping,” the clock and all other inputs are ignored. To wake up the device, ZZ must be returned LOW. This permits the input registers and clock to respond to inputs. It is recommended that users plan for four clock cycles to go into sleep mode and four clocks to emerge from sleep mode to ensure no data is lost.

Figure 2. Standard Sync SRAM Design Utilizing GW and BWE

Figure 3. Standard Sync SRAM Design Without Direct Connection of BE Signals to BW Signals
Converting Existing Designs to Accommodate New Functions

Figure 4 shows the connections for original and new devices in x36 nonpipelined applications. The differences on pins (mode) can be ignored when using the Cypress devices in interleaved burst sequence operation. If linear burst is required, pin 31 must be connected to ground to enable use of new devices. It is recommended, however, that all connections shown in the "New Functionality" illustration be adhered to if multiple vendors’ devices will be used. Pin 88 (GW) may be connected differently than in the original design.

Pipelined applications differ only in the connection of FT (pin 14) if multiple vendor support is desirable. Specifically, FT should be tied to 3.3V to conform to the JEDEC standard.

Figure 5 shows the connections for original and new devices in x32 applications where x36 devices were the only available parts at the time. The same discussion as above applies except that pin 87 (formerly PDIS, now BWE) must revert from a 3.3V connection to a ground connection.

Non-PC Applications

Many non-PC applications use the devices in a different manner. For example, byte operations may not be required. In this case, all BW signals are tied together in designs employing the original functionality. For compatibility, GW should be tied HIGH and BWE tied LOW. In the new designs, GW can be used to reduce signal loading. GW would be used to control Writes while BWE and BWa through BWd would be tied HIGH. This reduces the control signal load from four to one for the Write control function.

Summary

This article provides information which will enable designers to convert existing designs to be compatible with functional enhancements to the Standard Sync SRAM architecture.

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Figure 4. Converting from Original x36 Design to New Functionality

Figure 5. Converting from Original x36 Used as x32 to New Functionality
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