

August 1986 Revised March 2000

DM74LS194A 4-Bit Bidirectional Universal Shift Register

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load

Shift right (in the direction Q_A toward Q_D)

Shift left (in the direction Q_D toward Q_A)

Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, HIGH. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is HIGH and S1 is LOW. Serial data for this mode is entered at the shift-right data input. When S0 is LOW and S1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW.

Features

- Parallel inputs and outputs
- Four operating modes:

Synchronous parallel load

Right shift

Left shift

Do nothing

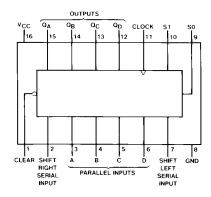
- Positive edge-triggered clocking
- Direct overriding clear

Ordering Code:

Order Number	Package Number	Number Package Description					
DM74LS194AM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow					
DM74LS194AN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide					

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

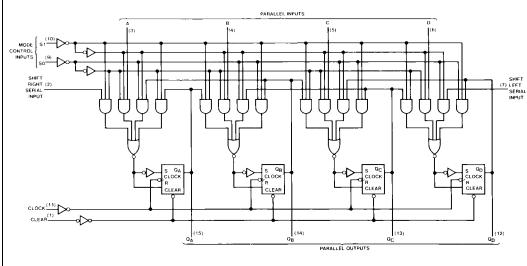


Function Table

Inputs						Outputs							
Clear	ode	Clock	Serial		Parallel			Q _A	Q _B	Q _C	Q_D		
Clear	S1	S0	CIUCK	Left	Right	Α	В	С	D	™ A	∝в	~C	∝ D
L	Х	Χ	Х	Х	Х	Х	Х	Х	Х	L	L	L	L
Н	Χ	Χ	L	Х	X	Х	Χ	Χ	Χ	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
Н	Н	Н	↑	Х	X	а	b	С	d	а	b	C	d
Н	L	Н	1	Х	Н	Х	Χ	Χ	Χ	Н	Q_{An}	Q_Bn	Q_Cn
Н	L	Н	1	Х	L	Х	Χ	Χ	Χ	L	Q_{An}	Q_Bn	Q_Cn
Н	Н	L	↑	Н	X	Х	Х	Χ	Χ	Q_{Bn}	Q_{Cn}	Q_Dn	Н
Н	Н	L	1	L	X	Χ	Χ	Χ		Q_{Bn}	Q_{Cn}	Q_{Dn}	L
Н	L	L	X	Х	X	Х	Χ	Χ	Χ	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

- $$\begin{split} &H = HIGH \ Level \ (steady \ state) \\ &L = LOW \ Level \ (steady \ state) \\ &X = Don't \ Care \ (any \ input, including \ transitions) \\ &\uparrow = Transition \ from \ LOW-to-HIGH \ level \ a, b, c, d = The \ level \ of \ steady \ state \ input \ at \ input \ at \ input \ at, B, C \ or \ D, \ respectively. \\ &Q_{A0}, \ Q_{B0}, \ Q_{C0}, \ Q_{D0} = The \ level \ of \ Q_A, \ Q_B, \ Q_C, \ or \ Q_D, \ respectively, before \ the \ indicated \ steady \ state \ input \ conditions \ were \ established. \\ &Q_{An}, \ Q_{Bn}, \ Q_{Cn}, \ Q_{Dn} = The \ level \ of \ Q_A, \ Q_B, \ Q_C, \ respectively, before \ the \ most-recent \ \uparrow \ transition \ of \ the \ clock. \end{split}$$

Logic Diagram



Absolute Maximum Ratings(Note 1)

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range $0^{\circ}\text{C to } +70^{\circ}\text{C}$ Storage Temperature Range $-65^{\circ}\text{C to } +150^{\circ}\text{C}$

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Paramet	Min	Nom	Max	Units		
V _{CC}	Supply Voltage	4.75	5	5.25	V		
V _{IH}	HIGH Level Input Voltage		2			V	
V _{IL}	LOW Level Input Voltage				0.8	V	
I _{OH}	HIGH Level Output Currer			-0.4	mA		
I _{OL}	LOW Level Output Curren			8	mA		
f _{CLK}	Clock Frequency (Note 2)	0		25	MHz		
	Clock Frequency (Note 3)	0		20	IVITZ		
t _W	Pulse Width	Clock	20				
	(Note 4)	Clear	20			ns	
t _{SU}	Setup Time	Mode	30				
	(Note 4)	Data	20			ns	
t _H	Hold Time (Note 4)	0			ns		
t _{REL}	Clear Release Time (Note	25			ns		
T _A	Free Air Operating Tempe	0		70	°C		

Note 2: $C_L = 15 \text{ pF}, T_A = 25^{\circ}\text{C} \text{ and } V_{CC} = 5\text{V}.$

Note 3: C_L = 50 pF, R_L = 2 $k\Omega,\,T_A$ = 25°C and V_{CC} = 5V.

Note 4: $T_A = 25^{\circ}C$ and $V_{CC} = 5V$.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units	
V _I	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$			-1.5	V	
V _{OH}	HIGH Level	V _{CC} = Min, I _{OH} = Max	2.7	3.4		V	
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$	2.7	5.4		v	
V _{OL}	LOW Level	V _{CC} = Min, I _{OL} = Max		0.35	0.5		
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$		0.55	0.5	V	
		I _{OL} = 4 mA, V _{CC} = Min			0.4		
T _I	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 7V$			0.1	mA	
I _{IH}	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.7V$			20	μΑ	
I _{IL}	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-0.4	mA	
Ios	Short Circuit Output Current	V _{CC} = Max (Note 6)	-20		-100	mA	
I _{CC}	Supply Current	V _{CC} = Max (Note 7)		15	23	mA	

Note 5: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^{\circ}C$

Symbol	Parameter	From (Input)	C _L = 50 pF	Units	
		To (Output)	Min	Max	Oilles
f _{MAX}	Maximum Clock Frequency		20		MHz
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		26	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		35	ns
t _{PHL}	Propagation Delay Time HIGH-to-LOW Output	Clear to Any Q		38	ns

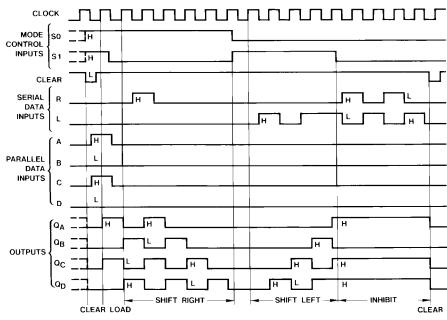
Note 8: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

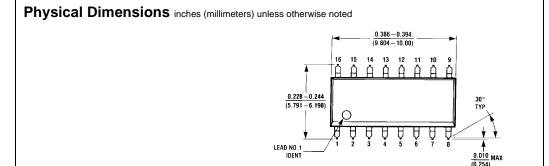
Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

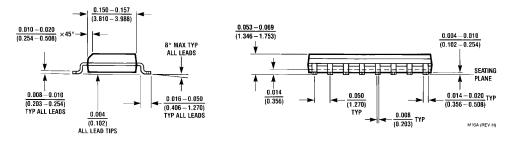
Note 10: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Timing Diagram

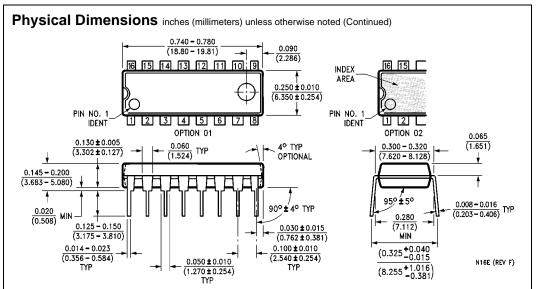








16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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