

# SN5470, SN7470 AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

SDLS116 - DECEMBER 1983 - REVISED MARCH 1988

- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

## description

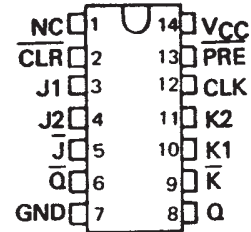
These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and  $\bar{Q}$  outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

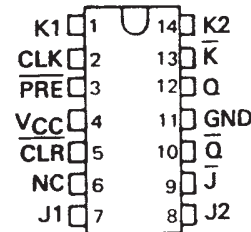
These flip-flops are ideally suited for medium-to-high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

The SN5470 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7470 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN5470 . . . J PACKAGE  
SN7470 . . . N PACKAGE  
(TOP VIEW)

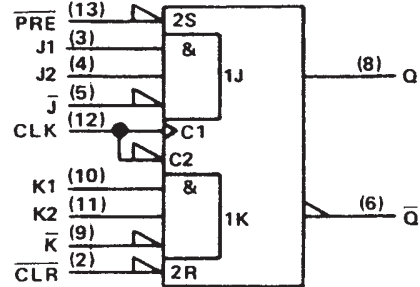


SN5470 . . . W PACKAGE  
(TOP VIEW)



NC - No internal connection

## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages only.

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	L	X	X	H	L
H	L	L	X	X	L	H
L	L	X	X	X	L†	L†
H	H	↑	L	L	Q <sub>0</sub>	Q <sub>0</sub>
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q <sub>0</sub>	Q <sub>0</sub>

If inputs J and K are not used, they must be grounded. Preset or clear function can occur only when the clock input is low.

†This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

## positive logic

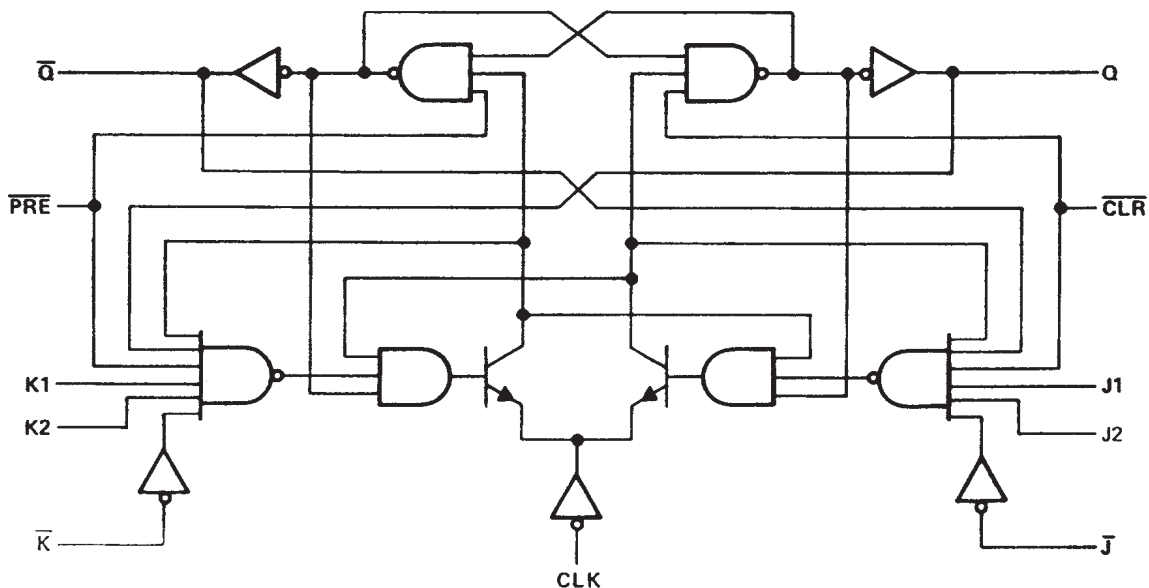
$$J = J1 \cdot J2 \cdot \bar{J}$$

$$K = K1 \cdot K2 \cdot \bar{K}$$

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**FLIP-FLOPS WITH PRESET AND CLEAR**

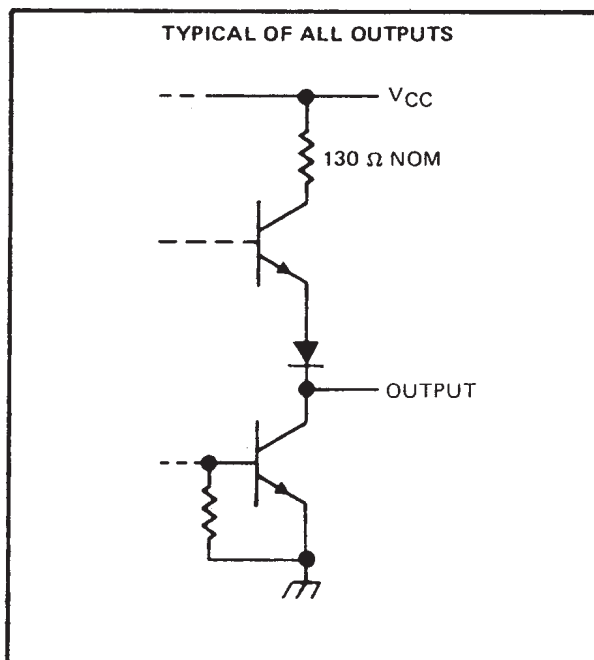
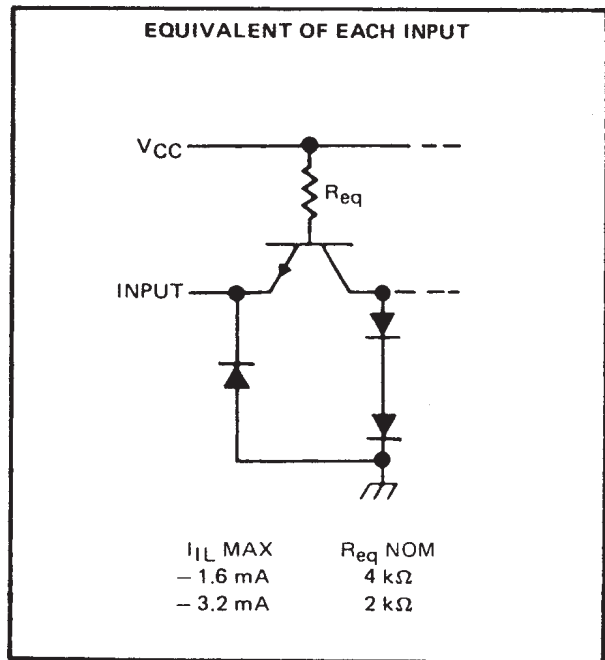
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**logic diagram (positive logic)**



'70-GATED J-K WITH CLEAR AND PRESET

**schematics of input and outputs**



# SN5470, SN7470 AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	.7 V
Input voltage .....	5.5 V
Operating free-air temperature: SN5470 .....	– 55°C to 125°C
SN7470 .....	.0°C to 70°C
Storage temperature range .....	– 65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

## recommended operating conditions

	SN5470			SN7470			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage	0.8			0.8			V
$I_{OH}$ High-level output current	– 0.4			– 0.4			mA
$I_{OL}$ Low-level output current	16			16			mA
$t_w$ Pulse duration	CLK high		20	20		ns	
	CLK low		30	30			
	PRE or CLR low		25	25			
$t_{su}$ Setup time before CLK $\uparrow$	20			20			ns
$t_h$ Hold time-Data after CLK $\uparrow$	5			5			ns
$T_A$ Operating free-air temperature	– 55		125	0		70	°C

†‡ The arrow indicates the edge of the clock pulse used for reference:  $\uparrow$  for the rising edge,  $\downarrow$  for the falling edge.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5470			SN7470			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$	– 1.5			– 1.5			V
$V_{OH}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$	1			1			mA
$I_{IH}$	PRE or CLR	80			80			$\mu\text{A}$
	All other	40			40			
$I_{IL}$	PRE or CLR†	– 3.2			– 3.2			mA
	All other	– 1.6			– 1.6			
$I_{OS}\S$	$V_{CC} = \text{MAX}$	– 20		– 57	– 18		– 57	mA
$I_{CC}$	$V_{CC} = \text{MAX},$ See Note 2		13	26		13	26	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§Not more than one output should be shorted at a time.

†Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is at 4.5 V.

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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see note 3)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\max}$			$R_L = 400\ \Omega$ , $C_L = 15\ \text{pF}$	20	35		MHz
$t_{\text{PLH}}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{\text{Q}}$				50	ns
$t_{\text{PHL}}$						50	ns
$t_{\text{PLH}}$	CLK	Q or $\overline{\text{Q}}$			27	50	ns
$t_{\text{PHL}}$					18	50	ns

†  $f_{\max}$  = maximum clock frequency;  $t_{\text{PLH}}$  = propagation delay time, low-to-high level output;  
 $t_{\text{PHL}}$  = propagation delay time, high-to-low level output.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN5470J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SN7470N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN7470N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SNJ5470J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ5470J	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
SNJ5470W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI
SNJ5470W	OBSOLETE	CFP	W	14		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

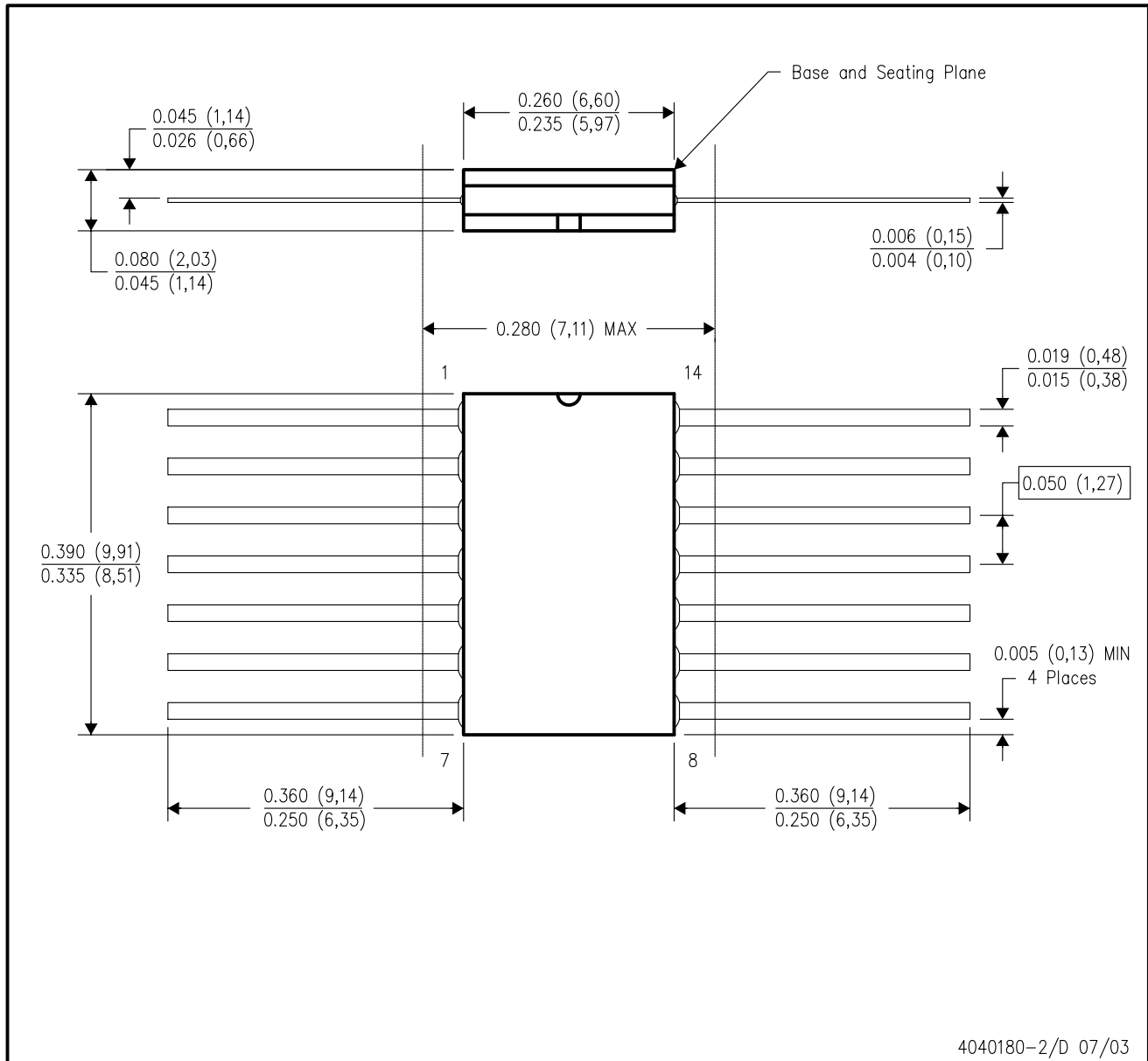


4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.



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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265