

## SNx4HC595 8-Bit Shift Registers With 3-State Output Registers

### 1 Features

- 8-Bit Serial-In, Parallel-Out Shift
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Low Power Consumption: 80- $\mu$ A (Maximum)  $I_{CC}$
- $t_{pd} = 13$  ns (Typical)
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current: 1  $\mu$ A (Maximum)
- Shift Register Has Direct Clear
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Network Switches
- Power Infrastructure
- LED Displays
- Servers

### 3 Description

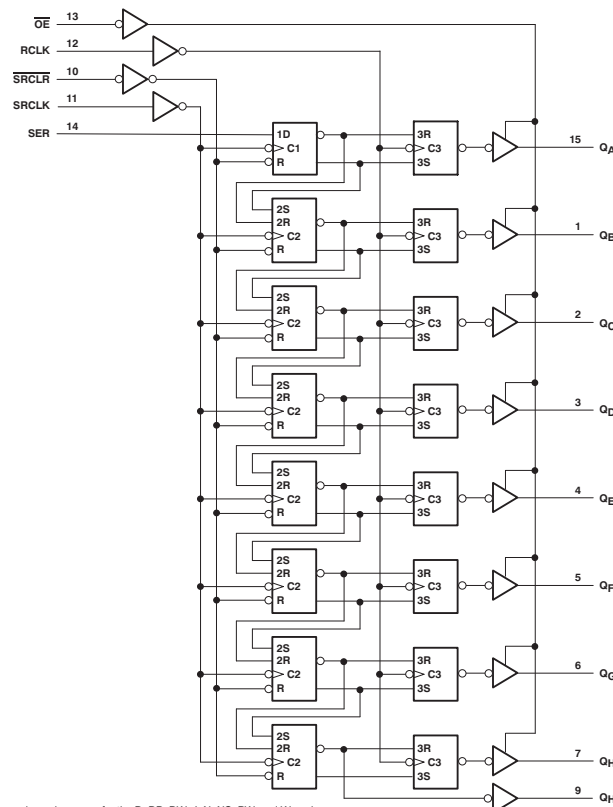
The SNx4HC595 devices contain an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage register. The shift register has a direct overriding clear (SRCLR) input, serial (SER) input, and serial outputs for cascading. When the output-enable ( $\overline{OE}$ ) input is high, the outputs are in the high-impedance state.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54HC595	LCCC (20)	8.89 mm x 8.89 mm
	CDIP (16)	21.34 mm x 6.92 mm
SN74HC595	PDIP (16)	19.31 mm x 6.35 mm
	SOIC (16)	9.90 mm x 3.90 mm
	SOIC (16)	10.30 mm x 7.50 mm
	SSOP (16)	6.20 mm x 5.30 mm
	TSSOP (16)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Logic Diagram (Positive Logic)



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

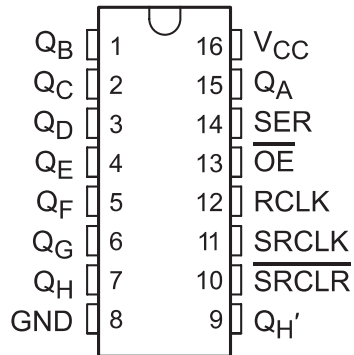
<b>Changes from Revision H (November 2009) to Revision I</b>	<b>Page</b>
• Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Deleted <i>Ordering Information</i> table. ....	<b>1</b>
• Added Military Disclaimer to <i>Features</i> list. ....	<b>1</b>

## 5 Device Comparison Table

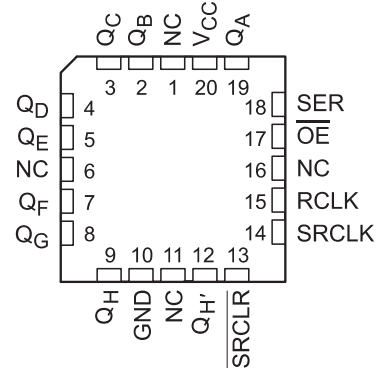
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54HC595FK	LCCC (20)	8.89 mm x 8.89 mm
SN54HC595J	CDIP (16)	21.34 mm x 6.92 mm
SN74HC595N	PDIP (16)	19.31 mm x 6.35 mm
SN74HC595D	SOIC (16)	9.90 mm x 3.90 mm
SN74HC595DW	SOIC (16)	10.30 mm x 7.50 mm
SN74HC595DB	SSOP (16)	6.20 mm x 5.30 mm
SN74HC595PW	TSSOP (16)	5.00 mm x 4.40 mm

## 6 Pin Configuration and Functions

D, N, NS, J, DB, or PW Package  
16-Pin SOIC, PDIP, SO, CDIP, SSOP, or TSSOP  
Top View



FK Package  
20-Pin LCCC  
Top View



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOIC, PDIP, SO, CDIP, SSOP, or TSSOP	LCCC		
GND	8	10	—	Ground Pin
$\overline{OE}$	13	17	I	Output Enable
$Q_A$	15	19	O	$Q_A$ Output
$Q_B$	1	2	O	$Q_B$ Output
$Q_C$	2	3	O	$Q_C$ Output
$Q_D$	3	4	O	$Q_D$ Output
$Q_E$	4	5	O	$Q_E$ Output
$Q_F$	5	7	O	$Q_F$ Output
$Q_G$	6	8	O	$Q_G$ Output
$Q_H$	7	9	O	$Q_H$ Output
$Q_{H'}$	9	12	O	$Q_{H'}$ Output
RCLK	12	14	I	RCLK Input
SER	14	18	I	SER Input
SRCLK	11	14	I	SRCLK Input
$\overline{SRCLR}$	10	13	I	$\overline{SRCLR}$ Input
NC	—	1	—	No Connection
		16		
		11		
		16		
$V_{CC}$	—	20	—	Power Pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		-0.5	7	V
I <sub>IK</sub>	Input clamp current <sup>(2)</sup>	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub>		±20	mA
I <sub>OK</sub>	Output clamp current <sup>(2)</sup>	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±35	mA
	Continuous current through V <sub>CC</sub> or GND			±70	mA
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54HC595			SN74HC595			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V		1.5	1.5			V
		V <sub>CC</sub> = 4.5 V		3.15	3.15			
		V <sub>CC</sub> = 6 V		4.2	4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V			0.5		0.5	V
		V <sub>CC</sub> = 4.5 V			1.35		1.35	
		V <sub>CC</sub> = 6 V			1.8		1.8	
V <sub>I</sub>	Input voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
Δt/Δv	Input transition rise or fall time <sup>(2)</sup>	V <sub>CC</sub> = 2 V			1000		1000	ns
		V <sub>CC</sub> = 4.5 V			500		500	
		V <sub>CC</sub> = 6 V			400		400	
T <sub>A</sub>	Operating free-air temperature	-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).
- (2) If this device is used in the threshold region (from V<sub>IL,max</sub> = 0.5 V to V<sub>IH,min</sub> = 1.5 V), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at t<sub>i</sub> = 1000 ns and V<sub>CC</sub> = 2 V does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AHCT595						UNIT
	D (SOIC)	DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)	
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	73	82	57	67	64	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

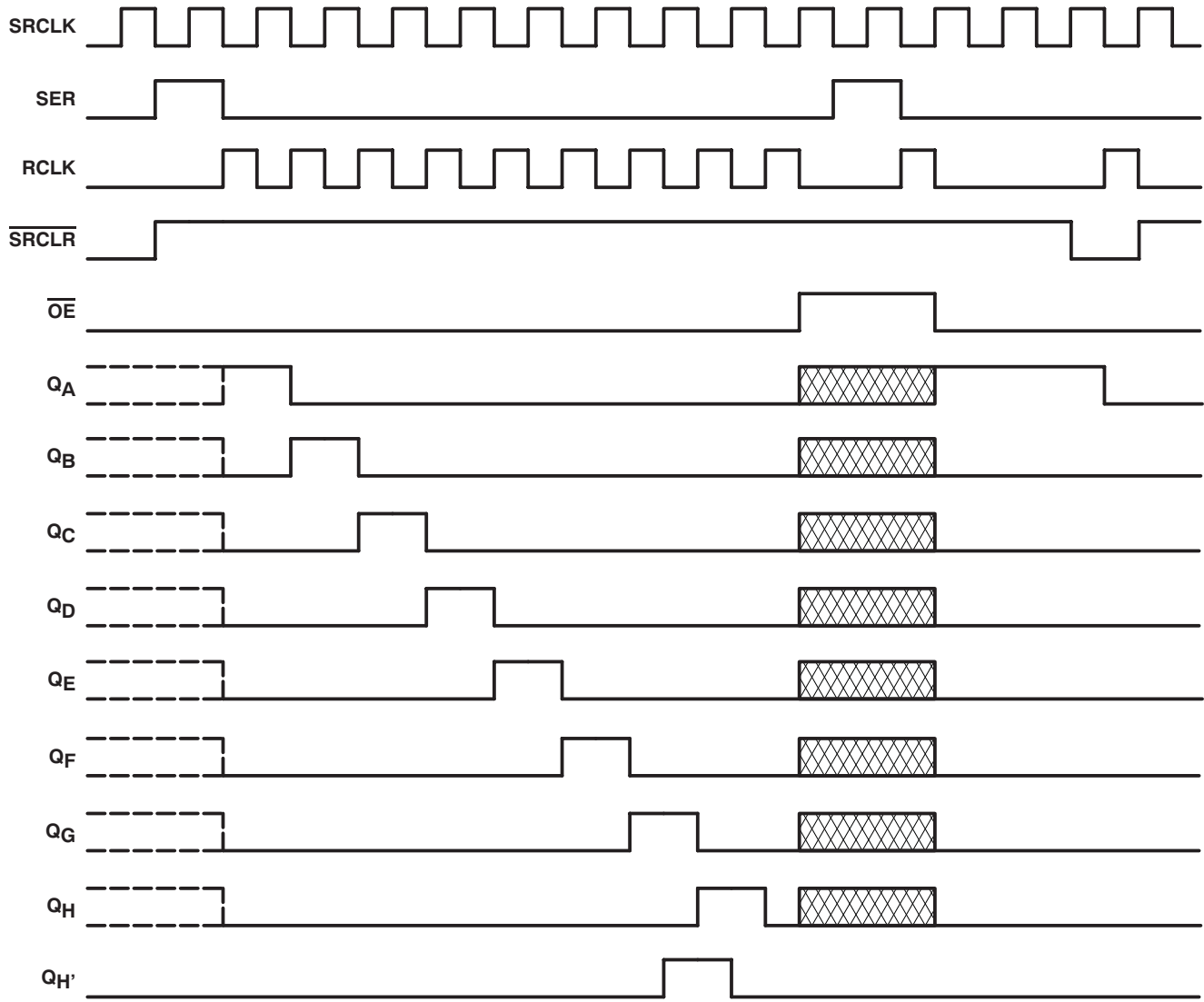
PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC595		SN74HC595		UNIT		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX			
$V_{OH}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V		
			4.5 V	4.4	4.499		4.4		4.4			
			6 V	5.9	5.999		5.9		5.9			
		4.5 V	$Q_H, I_{OH} = -4 \text{ mA}$		3.98	4.3		3.7			3.84	
			$Q_A - Q_H, I_{OH} = -6 \text{ mA}$		3.98	4.3		3.7			3.84	
			$Q_H, I_{OH} = -5.2 \text{ mA}$		5.48	5.8		5.2			5.34	
6 V	$Q_A - Q_H, I_{OH} = -7.8 \text{ mA}$		5.48	5.8		5.2		5.34				
$V_{OL}$	$V_I = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V	
			4.5 V		0.001	0.1		0.1		0.1		
			6 V		0.001	0.1		0.1		0.1		
		4.5 V	$Q_H, I_{OL} = 4 \text{ mA}$			0.17	0.26		0.4			0.33
			$Q_A - Q_H, I_{OL} = 6 \text{ mA}$			0.17	0.26		0.4			0.33
			$Q_H, I_{OL} = 5.2 \text{ mA}$			0.15	0.26		0.4			0.33
6 V	$Q_A - Q_H, I_{OL} = 7.8 \text{ mA}$			0.15	0.26		0.4		0.33			
$I_I$	$V_I = V_{CC}$ or 0	6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$		$\pm 1000$	nA		
$I_{OZ}$	$V_O = V_{CC}$ or 0, $Q_A - Q_H$	6 V		$\pm 0.01$	$\pm 0.5$		$\pm 10$		$\pm 5$	$\mu\text{A}$		
$I_{CC}$	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	$\mu\text{A}$		
$C_i$		2 V to 6 V		3	10		10		10	pF		

## 7.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC595		SN74HC595		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	6		4.2		5		MHz
		4.5 V	31		21		25		
		6 V	36		25		29		
t <sub>w</sub>	SRCLK or RCLK high or low	2 V	80	120	100	ns			
		4.5 V	16	24	20				
		6 V	14	20	17				
	$\overline{\text{SRCLR}}$ low	2 V	80	120	100				
		4.5 V	16	24	20				
		6 V	14	20	17				
t <sub>SU</sub>	SER before SRCLK↑	2 V	100	150	125	ns			
		4.5 V	20	30	25				
		6 V	17	25	21				
	SRCLK↑ before RCLK↑ <sup>(1)</sup>	2 V	75	113	94				
		4.5 V	15	23	19				
		6 V	13	19	16				
	$\overline{\text{SRCLR}}$ low before RCLK↑	2 V	50	75	65				
		4.5 V	10	15	13				
		6 V	9	13	11				
	$\overline{\text{SRCLR}}$ high (inactive) before SRCLK↑	2 V	50	75	60				
		4.5 V	10	15	12				
		6 V	9	13	11				
t <sub>h</sub>	Hold time, SER after SRCLK↑	2 V	0	0	0	ns			
		4.5 V	0	0	0				
		6 V	0	0	0				

(1) This set-up time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.




NOTE:  implies that the output is in 3-State mode.

Figure 1. Timing Diagram



## 7.7 Switching Characteristics

Over recommended operating free-air temperature range.

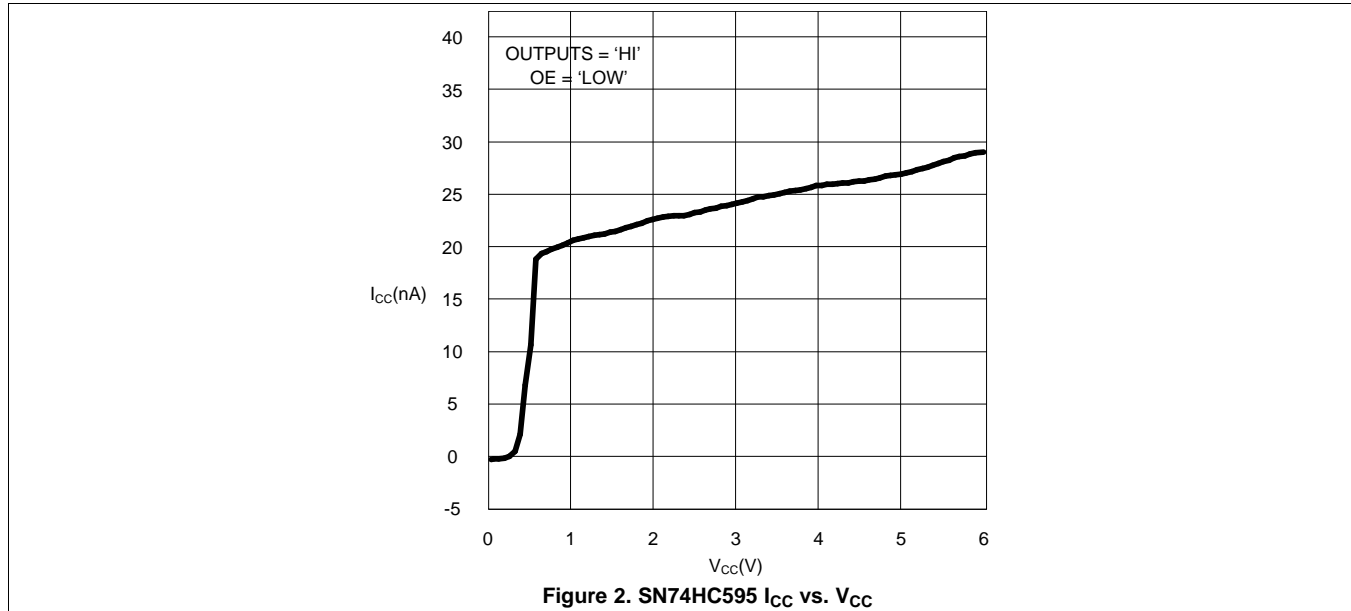
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC595		SN74HC595		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			50 pF	2 V	6	26		4.2		5	MHz	
				4.5 V	31	38		21		25		
				6 V	36	42		25		29		
t <sub>pd</sub>	SRCLK	Q <sub>H'</sub>	50 pF	2 V		50	160		240		200	ns
				4.5 V		17	32		48		40	
				6 V		14	27		41		34	
	RCLK	Q <sub>A</sub> – Q <sub>H</sub>	50 pF	2 V		50	150		225		187	
				4.5 V		17	30		45		37	
				6 V		14	26		38		32	
t <sub>PHL</sub>	$\overline{\text{SRCLR}}$	Q <sub>H'</sub>	50 pF	2 V		51	175		261		219	ns
				4.5 V		18	35		52		44	
				6 V		15	30		44		37	
t <sub>en</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> – Q <sub>H</sub>	50 pF	2 V		40	150		255		187	ns
				4.5 V		15	30		45		37	
				6 V		13	26		38		32	
t <sub>dis</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> – Q <sub>H</sub>	50 pF	2 V		42	200		300		250	ns
				4.5 V		23	40		60		50	
				6 V		20	34		51		43	
t <sub>t</sub>		Q <sub>A</sub> – Q <sub>H</sub>	50 pF	2 V		28	60		90		75	ns
				4.5 V		8	12		18		15	
				6 V		6	10		15		13	
		Q <sub>H'</sub>	50 pF	2 V		28	75		110		95	
				4.5 V		8	15		22		19	
				6 V		6	13		19		16	
t <sub>pd</sub>	RCLK	Q <sub>A</sub> – Q <sub>H</sub>	150 pf	2 V		60	200		300		250	ns
				4.5 V		22	40		60		50	
				6 V		19	34		51		43	
t <sub>en</sub>	$\overline{\text{OE}}$	Q <sub>A</sub> – Q <sub>H</sub>	150 pf	2 V		70	200		298		250	ns
				4.5 V		23	40		60		50	
				6 V		19	34		51		43	
t <sub>t</sub>		Q <sub>A</sub> – Q <sub>H</sub>	150 pf	2 V		45	210		315		265	ns
				4.5 V		17	42		63		53	
				6 V		13	36		53		45	

## 7.8 Operating Characteristics

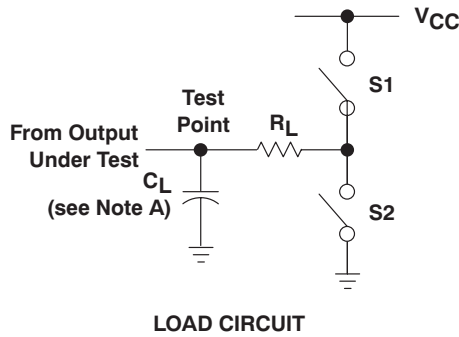
 T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load	400	pF

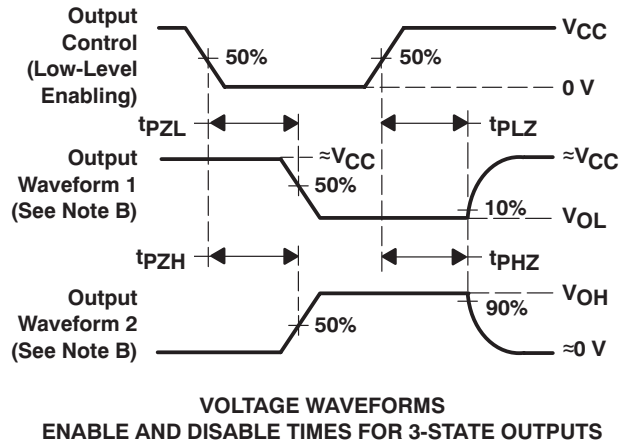
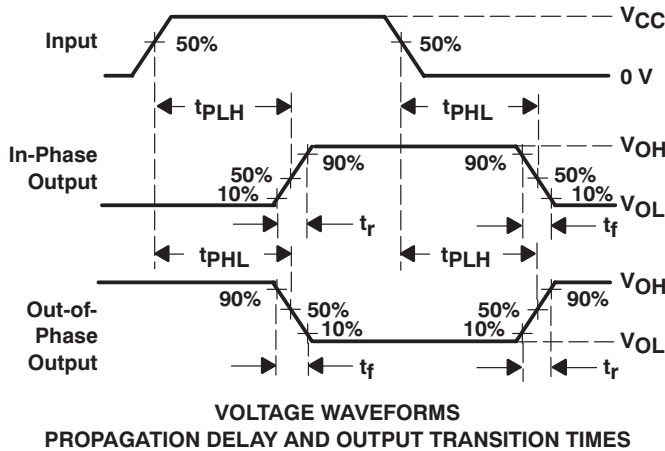
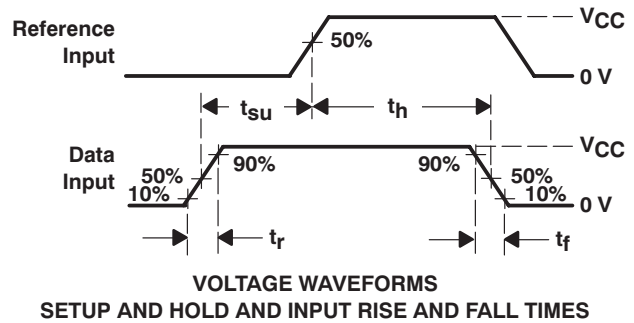
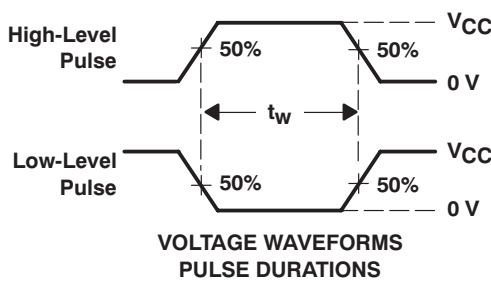
## 7.9 Typical Characteristics



## 8 Parameter Measurement Information



PARAMETER	$R_L$	$C_L$	S1	S2	
$t_{en}$	$t_{pZH}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
	$t_{pZL}$			Closed	Open
$t_{dis}$	$t_{pHZ}$	1 k $\Omega$	50 pF	Open	Closed
	$t_{pLZ}$			Closed	Open
$t_{pd}$ or $t_t$		50 pF or 150 pF	Open	Open	



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - E. The outputs are measured one at a time, with one input transition per measurement.
  - F.  $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
  - G.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
  - H.  $t_{pLH}$  and  $t_{pHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

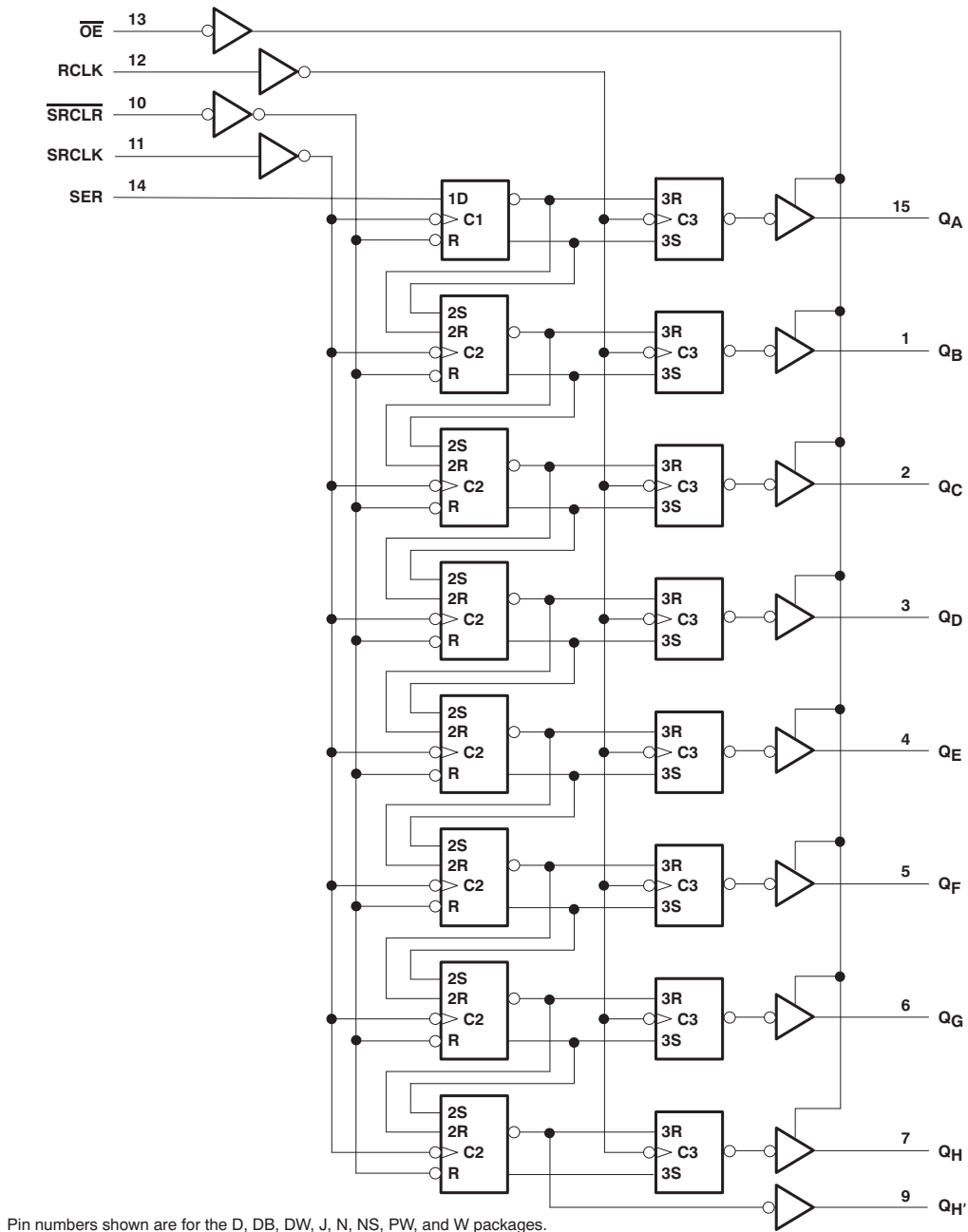
## 9 Detailed Description

### 9.1 Overview

The SNx4HC595 is part of the HC family of logic devices intended for CMOS applications. The SNx4HC595 is an 8-bit shift register that feeds an 8-bit D-type storage register.

Both the shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

### 9.2 Functional Block Diagram



**Figure 4. Logic Diagram (Positive Logic)**

### 9.3 Feature Description

The SNx4HC595 devices are 8-bit Serial-In, Parallel-Out Shift Registers. They have a wide operating current of 2 V to 6 V, and the high-current 3-state outputs can drive up to 15 LSTTL Loads. The devices have a low power consumption of 80- $\mu$ A (Maximum)  $I_{CC}$ . Additionally, the devices have a low input current of 1  $\mu$ A (Maximum) and a  $\pm 6$ -mA Output Drive at 5 V.

### 9.4 Device Functional Modes

Table 1 lists the functional modes of the SNx4HC595 devices.

**Table 1. Function Table**

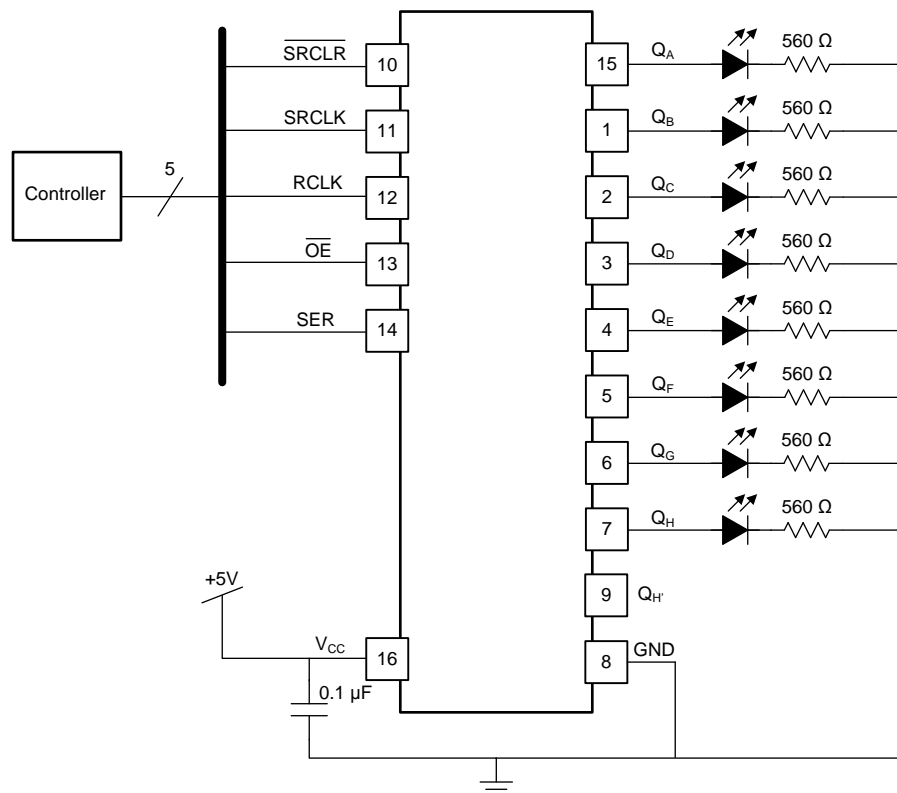
INPUTS					FUNCTION
SER	SRCLK	SRCLR	RCLK	$\overline{OE}$	
X	X	X	X	H	Outputs $Q_A - Q_H$ are disabled.
X	X	X	X	L	Outputs $Q_A - Q_H$ are enabled.
X	X	L	X	X	Shift register is cleared.
L	$\uparrow$	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	$\uparrow$	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	$\uparrow$	X	Shift-register data is stored in the storage register.

## 10 Application and Implementation

### 10.1 Application Information

The SNx4HC595 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

### 10.2 Typical Application



**Figure 5. Typical Application Schematic**

#### 10.2.1 Design Requirements

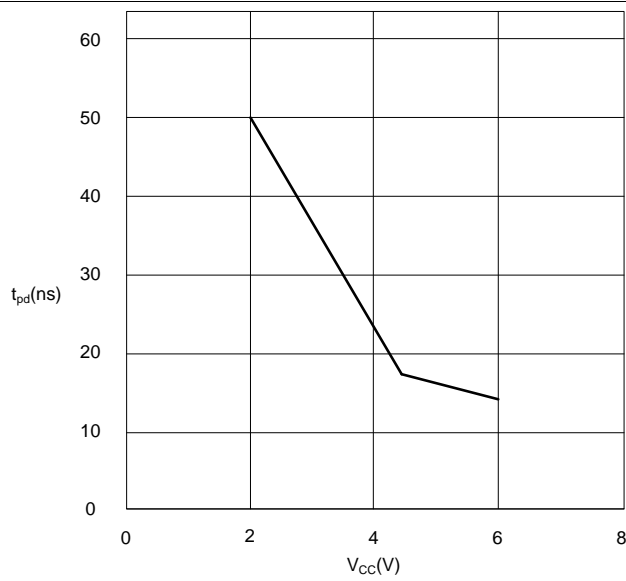
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

- Recommended input conditions
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$
- Recommend output conditions
  - Load currents should not exceed 35 mA per output and 70 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

**Typical Application (continued)**

**10.2.3 Application Curves**



**Figure 6. SN75HC595  $t_{pd}$  vs.  $V_{CC}$**

## 11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{f}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{f}$  or 0.022  $\mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{f}$  and a 1  $\mu\text{f}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 7](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 12.2 Layout Example



**Figure 7. Layout Diagram**



## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC595	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74HC595	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.