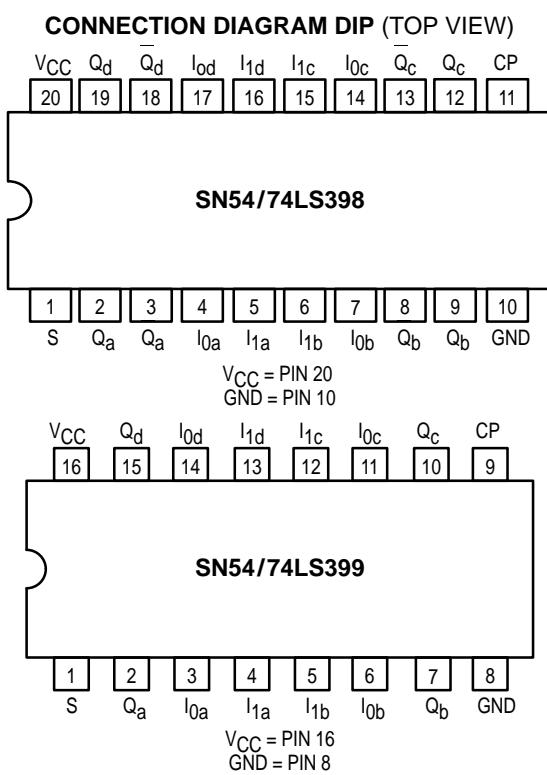


QUAD 2-PORT REGISTER

The SN54/74LS398 and SN54/74LS399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The SN54/74LS398 features both Q and \bar{Q} inputs, while the SN54/74LS399 has only Q outputs.

- Select From Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complemented Outputs on SN54/74LS398
- Input Clamp Diodes Limit High-Speed Termination Effects



PIN NAMES

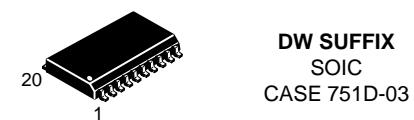
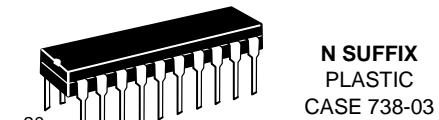
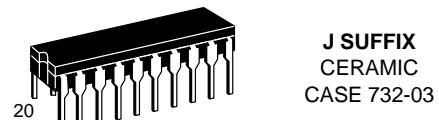
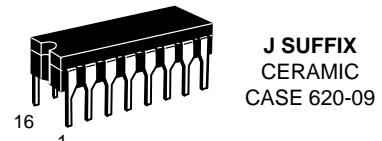
		LOADING (Note a)	
		HIGH	LOW
S	Common Select Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
I _{0a} -I _{0d}	Data Inputs From Source 0	0.5 U.L.	0.25 U.L.
I _{1a} -I _{1d}	Data Inputs From Source 1	0.5 U.L.	0.25 U.L.
Q _a -Q _d	Register True Outputs (Note b)	10 U.L.	5 (2.5) U.L.
Q _a -Q _d	Register Complementary Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

SN54/74LS398
SN54/74LS399

QUAD 2-PORT REGISTER
LOW POWER SCHOTTKY

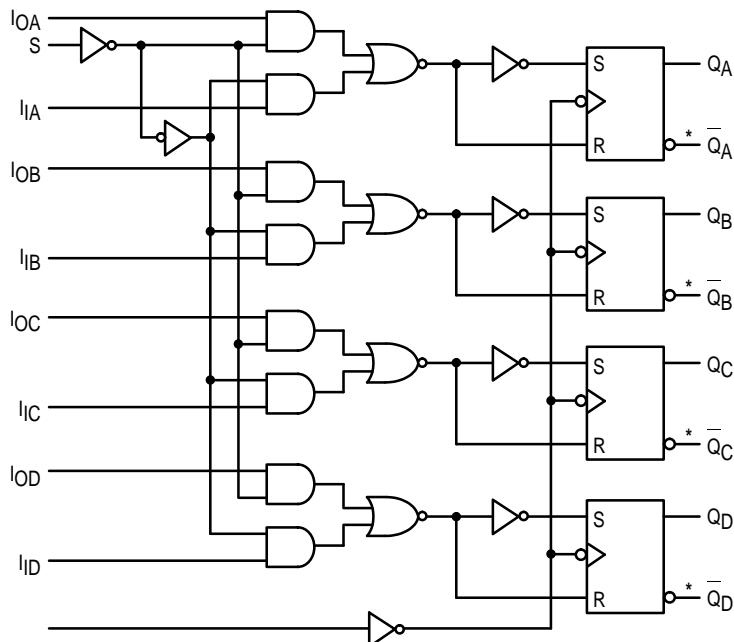


ORDERING INFORMATION

SN54LSXXXJ Ceramic
 SN74LSXXXN Plastic
 SN74LSXXXDW SOIC
 SN74LSXXXD SOIC

SN54/74LS398 • SN54/74LS399

FUNCTIONAL BLOCK DIAGRAM



* SN54/74LS398 only

FUNCTIONAL DESCRIPTION

The SN54/74LS398 and SN54/74LS399 are high-speed Quad 2-Port Registers. They select four bits of data from two sources (Ports) under the control of a common Select Input (S). The selected data is transferred to a 4-Bit Output Register synchronous with the LOW-to-HIGH transition of the Clock in-

put (CP). The 4-Bit RS type output register is fully edge-triggered. The Data inputs (I) and Select inputs (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The SN54/74LS398 has both Q and \bar{Q} Outputs available.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I ₀	I ₁	Q	\bar{Q}^*
I	I	X	L	H
I	h	X	H	L
h	X	I	L	H
h	X	h	H	L

*SN54/74LS398 only

I = LOW Voltage Level one setup time prior to the LOW-to-HIGH clock transition
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH clock transition

L = LOW Voltage Level

H = HIGH Voltage Level

X = Immaterial

SN54/74LS398 • SN54/74LS399

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage		54 74	4.5 4.75	5.0 5.0	V
T _A	Operating Ambient Temperature Range		54 74	-55 0	25 25	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA
		74	0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current		20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
			0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current		-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)	-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current		13	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, Clock to Output Q		18 21	27 32	ns	V _{CC} = 5.0 V C _L = 15 pF

SN54/74LS398 • SN54/74LS399

AC SETUP REQUIREMENTS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions $V_{CC} = 5.0 \text{ V}$
		Min	Typ	Max		
t_W	Clock Pulse Width	20			ns	
t_S	Data Setup Time	25			ns	
t_S	Select Setup Time	45			ns	
t_h	Hold Time, Any Input	0			ns	

DEFINITIONS OF TERMS

SETUP TIME(t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME(t_h) — is defined as the minimum time following

the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

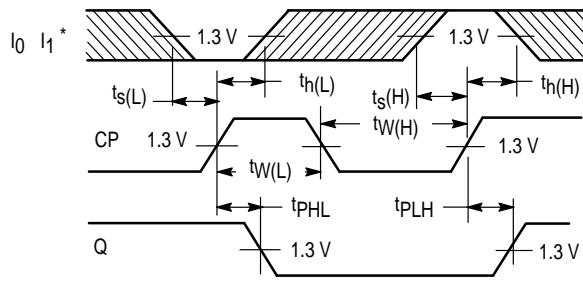


Figure 1

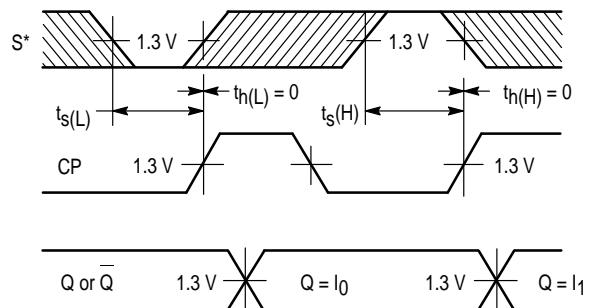


Figure 2

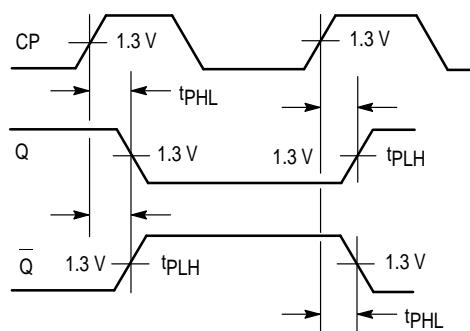


Figure 3

*The shaded areas indicate when the input is permitted to change for predictable output performance.