EE 202L
Class #8
Subject to **Negative Feedback** …

\[ v^+ \approx v^- \]

\[ v^+ - v^- = \frac{v_{\text{out}}}{A_{\text{vd}}} A_{\text{vd}} \to \infty \approx 0 \]

\[ i^+ \approx 0 \quad i^- \approx 0 \]

**Black-Box Op-Amp Rules**

\[ V^- \leq v_{\text{out}} \leq V^+ \]
Review Problem

Determine Node Voltages $v_x$ and $v_y$
Exercise 1

Build Me

V_{out} = ?

LM741

Voltmeter

100 kΩ

1 kΩ
\[ v^+ \text{ (outside)} = 0 \quad \rightarrow \quad v^+ \text{ (inside)} = v_{os} \]
Offset Source and Adjustment

Symmetry?
Exercise 2

Put Ice on Me

\[ V_{os} \text{ Variation?} \]
Digital to Analog Conversion

Why?
- Analog World
- Music, Video, Actuators, …

Given Bits \( b_1, b_2, b_3, \ldots \)

\[
b_x = \begin{cases} 
1 \\
0 
\end{cases}
\]

\[
v_{out} = V_{ref} \left( b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots \right)
\]
$$b_x = \begin{cases} 
1 & \text{switch closed} \\
0 & \text{switch open} 
\end{cases}$$

Example: 101

$$\frac{5V_{ref}}{8}$$

N Bits:
2\(^N\) Resistors
2 x (2\(^N\) - 1) Switches

High Speed!
4-Bit Current-Mode DAC

\[ b_x = \begin{cases} 
1 & \text{switch closed} \\
0 & \text{switch open}
\end{cases} \]

\[ v_{out} = \frac{V_{ref}}{R} \left( 2^{-1} b_1 + 2^{-2} b_2 + 2^{-3} b_3 + 2^{-4} b_4 \right) \]

\[ i' = b_1 i_1 + b_2 i_2 + b_3 i_3 + b_4 i_4 \]

\[ v_{out} = i' R_f \]
Integrated-Circuit Resistors

R Specified in Ohms/Square \( \Omega/\square \)

Large-Value IC Resistors Are Physically Large (Long)
4-Bit R-2R Current-Mode DAC

\[ i_{ref} = \frac{0 - (-V_{ref})}{R} \]

\[ i_1 = \frac{V_{ref}}{2R} = i_{x1} \]

\[ i_2 = \frac{V_{ref}}{4R} = i_{x2} \]

etc.

N Bits:
2N + 1 Resistors
N Switches
4-Bit R-2R Current-Mode DAC

\[ v_{out} = \frac{V_{ref}}{R} \left( 2^{-1}b_1 + 2^{-2}b_2 + 2^{-3}b_3 + 2^{-4}b_4 \right)R_f \]

\[ i' = b_1i_1 + b_2i_2 + b_3i_3 + b_4i_4 \]

\[ b_x = \begin{cases} 
1 & \rightarrow \text{virtual ground} \\
0 & \rightarrow \text{ground} 
\end{cases} \]
4-Bit R-2R Voltage-Mode DAC

To Op-Amp Amplifier and Output

Example: 0100

\[ v_y = V_{ref} \left( \frac{3R \parallel 2R}{3R \parallel 2R + 2R} \right) = \frac{3V_{ref}}{8} \]

\[ v_x = v_y \left( \frac{R}{R + 2R} \right) = \frac{V_{ref}}{4} \]

\[ b_x = \begin{cases} 
1 & \rightarrow V_{ref} \\
0 & \rightarrow \text{ground} 
\end{cases} \]
Offset Error and Gain Error

Both Easily Adjusted to Zero

Offset Error

Gain Error
INL and DNL

Non-Adjustable - Critical Specifications

Integral Non-Linearity

Differential Non-Linearity
MX7245 Parallel-Input DAC (12 Bits)
MAX5231 Serial-Input DAC (12 Bits)

Offset Adjusts
### Table 1. Serial Data Format

<table>
<thead>
<tr>
<th>MSB</th>
<th>16-bits of serial data</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 Control Bits</td>
<td>MSB ... 12 Data Bits ... LSB</td>
<td>Sub-Bit</td>
</tr>
<tr>
<td>C2...C0</td>
<td>D11 ...</td>
<td>D0</td>
</tr>
</tbody>
</table>

### Table 2. Serial-Interface Programming Commands

<table>
<thead>
<tr>
<th>16-BIT SERIAL WORD</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 1 12-bit DAC data 0</td>
<td>Load input register A; DAC registers are unchanged.</td>
</tr>
<tr>
<td>0 1 0 12-bit DAC data 0</td>
<td>Load all DAC registers from the shift register (start up both DACs with new data, and load the input registers).</td>
</tr>
<tr>
<td>0 1 1 12-bit DAC data 0</td>
<td>Update both DAC registers from their respective input registers (start up both DACs with data previously stored in the input registers).</td>
</tr>
<tr>
<td>1 0 0 X X X X X X X</td>
<td>Load input register B; DAC registers are unchanged.</td>
</tr>
<tr>
<td>1 0 1 12-bit DAC data 0</td>
<td>Load input register B; all DAC registers are updated.</td>
</tr>
<tr>
<td>1 1 1 P1A P1B X X X X X X X</td>
<td>Shut down both DACs, respectively, according to bits P1A and P1B (see Table 3). Internal bias and reference remain active.</td>
</tr>
<tr>
<td>0 0 0 0 0 1 X X X X X</td>
<td>Update DAC register A from input register A (start up DAC A with data previously stored in input register A).</td>
</tr>
<tr>
<td>0 0 0 0 0 1 1 P1A P1B X X X X X</td>
<td>Full Power-Down: Power down the main bias generator and shut down both DACs, respectively, according to bits P1A and P1B (see Table 3).</td>
</tr>
<tr>
<td>0 0 0 0 1 0 1 X X X X X</td>
<td>Update DAC register B from input register B (start up DAC B with data previously stored in input register B).</td>
</tr>
<tr>
<td>0 0 0 0 1 1 0 P1A X X X X X</td>
<td>Shut down DAC A according to bit P1A (see Table 3).</td>
</tr>
<tr>
<td>0 0 0 1 1 1 0 1 P1B X X X X X</td>
<td>Shut down DAC B according to bit P1B (see Table 3).</td>
</tr>
<tr>
<td>0 0 0 1 0 0 0 X X X X X</td>
<td>Mode 0. DOUT clocked out on SCLK falling edge (default).</td>
</tr>
<tr>
<td>0 0 0 1 0 0 1 X X X X X</td>
<td>Mode 1. DOUT clocked out on SCLK rising edge.</td>
</tr>
</tbody>
</table>

X = Don’t care.

* S0 must be zero for proper operation.
MAX5231 INL and DNL Data