Lab 7 Part 3

Subpart 3

HINTs
Two TRAPS
WERE SET UP
One
or
multiple
Clocked
procedural blocks?
Any μP has

1000's of registers
So 1000's of clocked blocks?
Or
just 1 big clocked block?
If NSLs are disjoint and separate then both separate or combined clocked block(s) are possible.
Sample RTL code

2 Separate Clocked blocks

```verilog
// always @(negedge CLK) // due to write
begin : RegFile_Block
  if (WB_WRITE)
    begin
      reg_file[WBLB] <= WB_RD;
    end
  end
end

// always @(posedge CLK, negedge RSTB)
begin : Main_Clocked_Block // N
```
TRAP #1

Common error

1. Keep two separate always blocks

2. Code the max in one of the two.

```verilog
always @(negedge CLK) // due to writ
begin : Regfile_Block
  if (WB_WRITE)
  begin
    reg_file[WB_RA] <= WB_RD;
  end
end

always @(posedge CLK, negedge RSTB)
begin : Main_Clocked_Block // N
end
```
Golden rule:
Every non-blocking assignment in a clocked processes will result in a physical register!

```vhls
always @ (posedge CLK)
begin : NSL_SM_example
    D = D1 & D2;
    Q <= D;
end
```

```vhls
always @ (posedge CLK)
begin : NSL_SM_example
    D <= D1 & D2;
    Q <= D;
end
```
intermediate variables in a clocked block? Then, treat them as local and do not reference them from outside!

always @ (posedge CLK)
begin : NSL_SM_example
  D = D1 & D2;
  Q <= D;
end

always @ (posedge CLK)
begin : NSL_SM_example
  Q_inverted_D = ~ D;
end

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If you wanted this hardware, then code all NSL and both registers in one always block or code the **NSL separately** in a combinational block.

```verilog
always @ (posedge CLK)
begin : NSL_SM_example
    D = D1 & D2;
    Q <= D;
    Q_inverted_D = ~ D;
end

assign D = D1 & D2;

always @ (posedge CLK)
begin : SM_example
    Q <= D;
    Q_inverted_D = ~ D;
end
```

Separate NSL

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TRAP #2

Simple minded approach which has a flaw:

OK, I will code in one clocked process.

I will code WB stage logic at the end.

As WB stage is the last stage.
WB_RD is needed in

EX2 ➔ forwarding XMEX1

EX1 ➔ forwarding XMEX2

ID for IFRF
ORDER OF CODE:

Code WB_RD first and then

Code

These Three

next

EX2 \rightarrow \text{forwarding XMEX1}

EX1 \rightarrow \text{forwarding XMEX2}

ID for JFRF